Abstract

Moore’s Law keep driving advances in semiconductor process technology as projected more than 40 years ago: a twofold transistor density about every two years. These advances have fueled the evolution in processor microarchitecture. In the past we saw the transition from CISC to RISC, and then to superscalar organizations. More recently we are witnessing an increased emphasis on exploiting thread-level parallelism through the so-called multicore chips.

Multicore processors are more power-area-effective and more reliable than big single-core processors. Because of that, they have become common in all market segments, from high-end servers to desktop and mobile PCs, and industry’ roadmap is heading towards an increasing degree of threading in all segments. However, single-thread performance still matters a lot, and will continue to be a very important differentiating factor of future highly-threaded processors.

This talk will discuss about the importance of single-thread performance in the era of highly-threaded processors, and describe several approaches that are being investigated to provide competitive single-thread and multi-threaded performance in future processors.

Bio

Antonio González received his M.S. and Ph.D. degrees from the Universitat Politècnica de Catalunya (UPC), in Barcelona, Spain. He is the founding director of the Intel Barcelona Research Center, started in 2002, whose research focuses on new microarchitecture paradigms and code generation techniques for future microprocessors. Prior to this, he joined the faculty of the Computer Architecture Department of UPC in 1986, and became a Full Professor in 2002. He currently holds an adjunct Professor position at this department.

Antonio González has published over 250 papers, has given over 80 invited talks, has filed over 40 patents and has advised 15 PhD theses in the areas of computer architecture and compilers. He has been an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Architecture and Code Optimization, and Journal of Embedded Computing. He has served on over 100 program committees for international symposia in the field of computer architecture, including ISCA, MICRO, ASPLOS, HPCA, PACT, ICS, ISPASS, CASES and IPDPS. He has been program chair for ICS 2003, ISPASS 2003, MICRO 2004 and HPCA 2008, and general chair for MICRO 2008, among other symposia.